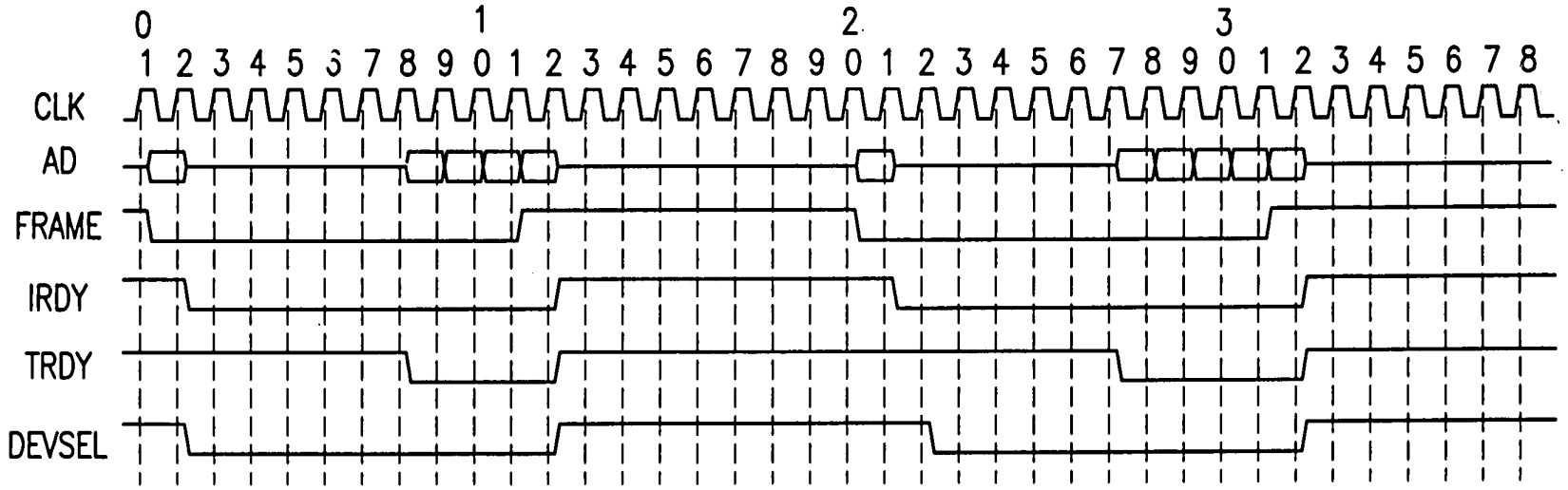

FIG. 1 (PRIOR ART)

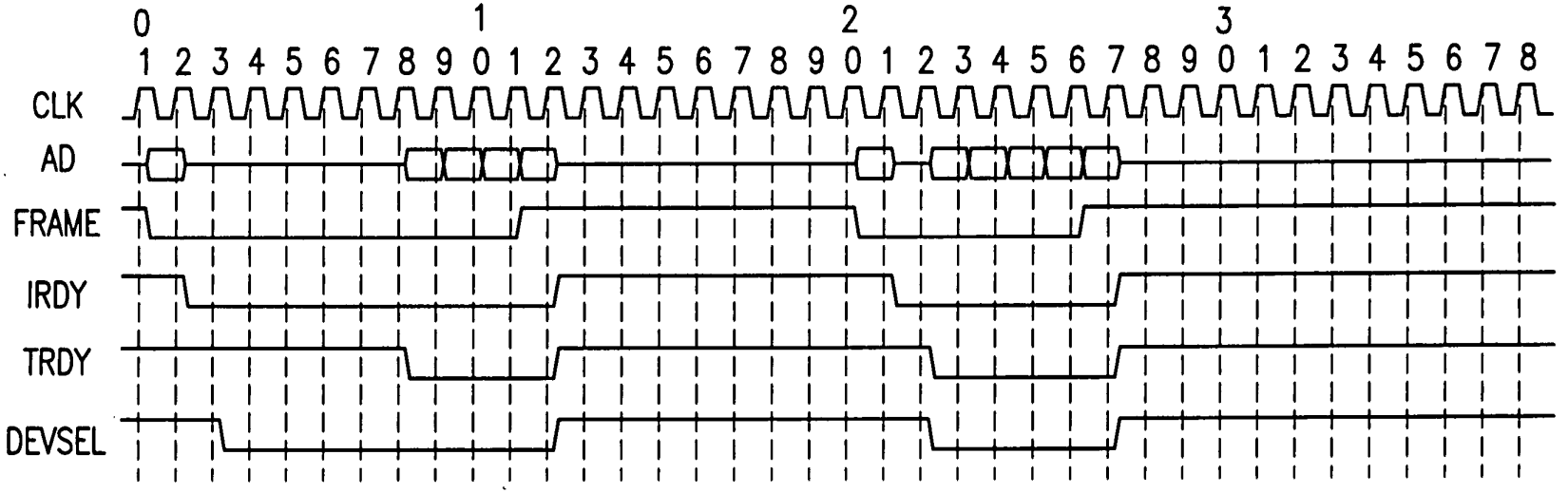

FIG. 3

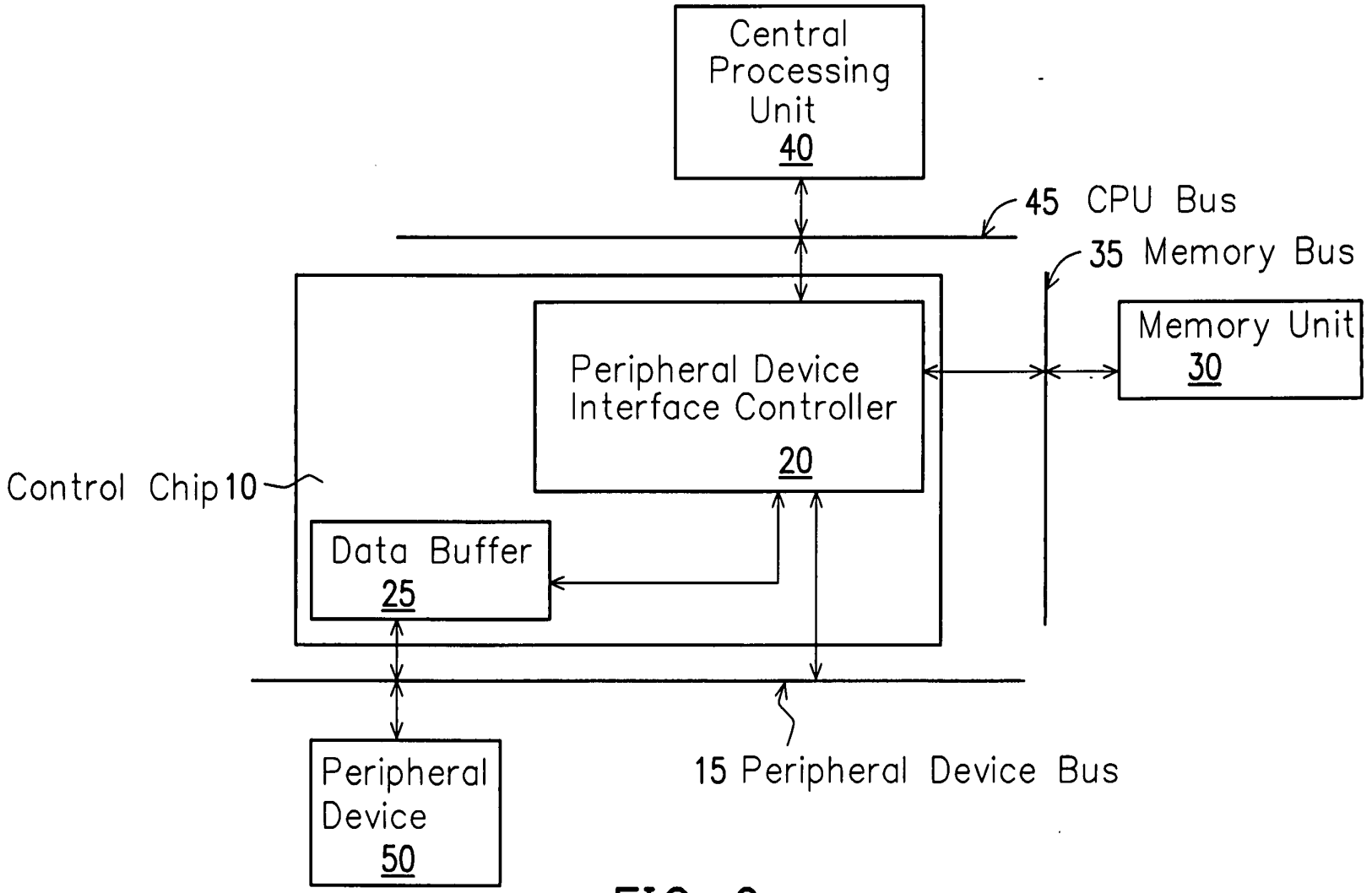
Central Processing Unit 40
45 CPU Bus
35 Memory Bus
Memory Unit 30
Peripheral Device Interface Controller 20
Control Chip 10
Data Buffer 25
Peripheral Device 50
15 Peripheral Device Bus

FIG. 2

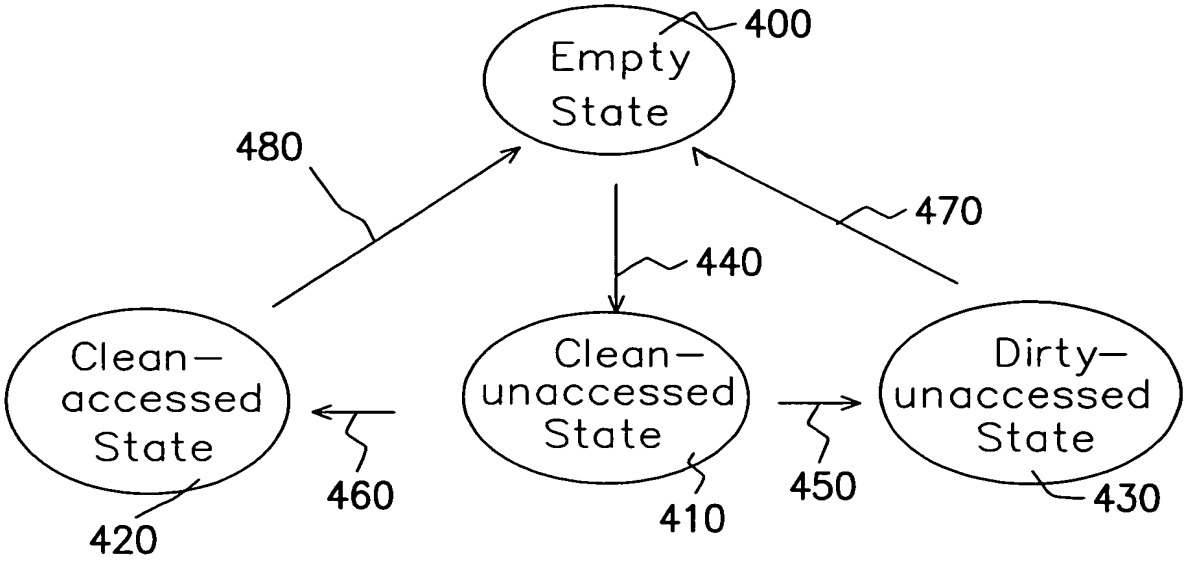
Empty State
400
480
470
440
Clean–accessed State
Clean–unaccessed State
Dirty–unaccessed State
460
450
420
410
430

FIG. 4

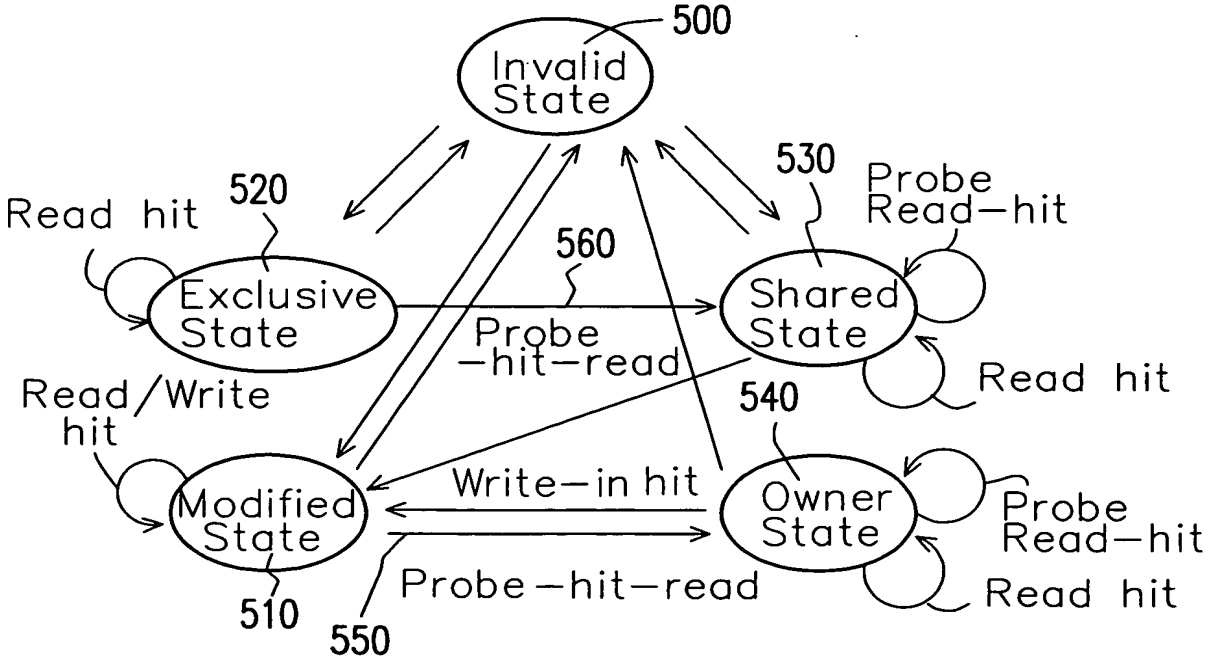
Invalid State
500
Read hit
520
530
Probe Read–hit
560
Exclusive State
Shared State
Probe –hit–read
Read hit
Read/Write hit
540
Write–in hit
Modified State
Owner State
Probe Read–hit
Read hit
Probe–hit–read
510
550

FIG. 5